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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,052	12/22/2000	Eugene D. Ham III	4015-808	1573

24112 7590 05/16/2007

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ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
05/16/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/747,052
Filing Date: December 22, 2000
Appellant(s): HAM, EUGENE D.

MAILED
MAY 16 2007
GROUP 2600

Michael D. Murphy
For Appellant

EXAMINER'S ANSWER

This is a Supplemental Examiner's Answer in response to Appeal Center Return, dated 24 April 2007, to correct some formality errors. The content of this Supplemental Examiner's Answer is the same as that of the previous Examiner's Answer in response to the appeal brief filed on October 26, 2006 appealing from the Office action mailed September 26, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. Claims 5-7, 13-16 and 18 under 35 U.S.C. 102(b) are withdrawn.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

US 5,909,148	Tanaka	June 01, 1999
US 6,353,647	Wilhelmsson et al.	March 05, 2002
US 5,619,543	Glass	April 08, 1997

(9) Grounds of Rejection

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 10, 11, 24-26, 32, and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (US 5,909,148).

- With regard claim 1, Tanaka discloses a method of generating an output signal from a phase-locked loop (PLL), comprising

determining successive phase difference values (Fig.1 elements 8 and 10) between a reference clock signal (Fig.2 element 6 output) and said output clock signal (Fig.1 element 9 output, where it is inherent that the NCO output can be taken as an output clock signal.);

filtering said successive phase difference values to generate successive control values (Fig.1 element 11);

controlling a frequency of said output clock signal based on said successive control values (Fig.1 element 13, 14, 15, 16, 101, and 102); and

adapting said filter used to filter said successive phase difference values based on average control values (Fig.1 element 13, 14, 15, 16, 101, and 102, and column 3 line 43 – column 4 line 23 and column 5 equation 8) determined from said successive control values.

- With regard claim 2, Tanaka further discloses detecting a trend in said average control values and determining a filter state based on said trend in said average control values (column 3 line 58 – column 4 line 18 and column 5 line 40 – column 6 line 25).
- With regard claim 3, Tanaka further discloses selecting a fast filter setting for said filter when said trend indicates that said average control values have not stabilized (column 3 line 58 – column 4 line 18 and column 5 line 40 – column 6 line 25).
- With regard claim 4, Tanaka further discloses a slow filter setting for said filter when said trend indicates that said average control values have stabilized (column 5 line 40 – column 6 line 25).
- With regard claim 10, which is a method of controlling a phase-locked loop (PLL) claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 11, which is a method of controlling a phase-locked loop (PLL) claim related to claims 3 and 4, all limitation is contained in claims 3 and 4. The explanation of all the limitation is already addressed in the above paragraph.

- With regard claim 24, Tanaka discloses a controllable oscillator (Fig.1 element 9) providing an output signal at a frequency proportionate to an oscillator control signal (Fig.1 element 11 output, g(nT)); and

  a phase detector providing a phase error signal (Fig.1 elements 8 and 10 and Fig.2 elements 4 and 10) by detecting a phase difference between an input signal and said output signal (Fig.1 element 6 output and element 9 output);

  an adjustable loop filter providing control values based on filtering said phase error signal (Fig.1 element 11);

  a control circuit providing the oscillator control signal (Fig.1 elements 9 and 11) responsive to said control values; and

  control logic to control a filter characteristic of said loop filter (Fig.1 elements 101 and 102, column 4 lines 1-18, and column 6 lines 1-25) based on an average control value determined from successive ones of said control values to minimize clock deviations in said output signal (Fig.1 elements 13-16, column 3 line 58 – column 4 line 18 and column 5 line 40 – column 6 line 25).

- In regard claim 25, Tanaka further discloses wherein said control logic is operable in one of a defined number of states (column 4 lines 3-18), and further wherein said control logic adjusts said filter characteristic of said loop filter based on a current state of said control logic (column 5 line 56 – column 6 line 25). It is inherent that the control logic is operable in at least one of the two states, lock state and unlock state (stable or unstable states). Tanaka's reference in column 5 line 56 – column 6 line 25 clearly describes how the filter 15 characteristics being adjust by the PLL controller 102 (control logic) based on its current state.

- In regard claim 26, Tanaka further discloses wherein said control logic transitions from a first state to a second state based on at least one characteristic of said average control values (column 6 lines 2-25).
- In regard claim 32, Tanaka further discloses wherein said loop filter comprises a digital loop filter adapted to output said control value in a digital format (Fig.1 element 11).

  Tanaka's reference describes that the A/D converter 2 converts the quasi-coherent orthogonal input signal as an analog signal into a digital signal (column 3 lines 46-48), thereafter, all processing steps are in digital form. It is inherent that the loop filter 11 is a digital loop filter (with digital output signal g(nT), formula 6 and 7).
- With regard claim 37, all limitation is contained in claim 26. The explanation of all the limitation is already addressed in the above paragraph.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 34, 35, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (US 5,909,148) in view of Wilhelmsson et al. (US 6,353,647).

- With regard claims 34 and 35, Tanaka discloses the claimed invention except for specifically teaching a DAC with input from a digital value generated from said loop filter and a VCO controlled by the DAC generated control viltage instead of a NCO 9 receiving a digital input value g(nT) from said loop filter 11. Wilhelmssons' reference shows that a DAC (Fig.12 element 3) with input from a digital value generated from said loop filter (Fig.12 element 44) and a VCO controlled by the DAC generated control viltage (Fig.12 element 9) is an equivalent structure known in the art. Therefore, because these two "the NCO" and "the DAC with VCO" were art-recognized equivalents at the time the Invention was made, one of ordinary skill in the art would have found it obvious to substitute (DAC and VCO) for (NCO).
- With respect to claim 39, Applicant does not define what the digital processor is in the claim and specification of the instant application. In specification page 11, line 11, teaches a digital loop filter 68. The output of the digital filter is submitted to the control logic 70. Since the control logic 70 processes the digital signal from the output of the digital loop filter 68, it is inherent that the control logic comprising a digital device for processing the input digital signal. The digital device for processing the digital signal is considered as a digital processor.

  With above interpretaion of the digital processor, Tanaka teaches a control logic (Fig.1 elements 13-16, 101 and 102) comprising a digital processor 14 to subtract a digital signal g(nT) and delayed digital signal g(nT-T) for subtraction operation or processing.

(10) Response to Argument

Claim Rejections under 35 USC § 102(e)

Independent Claims 1,10 and 24

1. Applicants' argument – Refer to pages 6-9 of the Appeal Brief.

(A) Summarized arguments under **All anticipation resections rely on improper claim construction:**

(a) The anticipation rejections of independent claims 1, 10, and 24 rely on a legally erroneous claim construction by the examiner. The applicant argues that the signal output by the Numerical Controlled Oscillator (NCO) 9 shown in Figure 1 of Tanaka is **the internal circuit feedback signal which is different from the PLL output signal claimed in claims 1, 10, and 24,** and argues that Applicant's claimed PLL output signals cannot be construed as encompassing internal circuit feedback signals generated by NCO 9 in Tanaka. Applicant has indicated its support in specification at p. 8, lines 14 — 15; and at p. 8, line 24 — p. 9, line 8. That is, the *"output clock signal from the PLL" of* claim *1,* the *"output signal generated by the PLL" of* claim 10, and the *"output signal from the PLL"* of claim 24 are output signals from the PLL at issue. For example, Figure 3 of the specification illustrates a radio head interface (RHI) 50 providing a timing output signal for a downstream radio transceiver (TRX) 52, and Figure 4 illustrates that a PLL module 62 in the RHI 50 generates that output clock signal for the TRX 52.

(b) Applicant argues that the claimed PLL output signal and the NCO 9 signal of Tanaka are not the same for claim interpretation purposes based on

"Figure C" at p. 6 of the Final Office Action. Figure C represents an arbitrary rearrangement of Figure 1 in Tanaka, where the examiner incorrectly re-labels the NCO 9 signal as an output frequency signal.

In conclusion, Applicant argues that with these plain teachings in the specification reinforcing the ordinary meaning of the output signal claimed in claims 1, 10, and 24, one of ordinary skill in the art would not interpret the claim output signal as encompassing the internal feedback signal from NCO 9 in Tanaka. Therefore, it is erroneous for the examiner to construe the claimed output signal as encompassing the internal feedback signal from NCO 9 in Tanaka because that construction is at direct odds with the requirement to construe a claim term "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364, 70 **USPQ2d 1827, 1834** (Fed. Cir. 2004). That is, the "broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." *In re Cortright,* ***165*** **F.3d** 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999).

Examiner's response – In response to applicant's argument as described above paragraph (a), Examiner notices that Applicant has confused his own design terms with respect to the **CLOCK OUTPUT** (output of the CONTER/DIVIDER 78, Fig.5) and the **output clock signal** (output of Oscillator 74).

With regard to the **CLOCK OUTPUT** , specification at p. 8, lines 14 — 15 and Figure 3 illustrates a radio head interface (RHI) 50 providing a timing output

signal for a downstream radio transceiver (TRX) 52, and at p. 8, line 24 — p. 9, line 8, and Figure 4 illustrates that a PLL module 62 in the RHI 50 generates that output clock signal for the TRX 52. Furthermore, in specification at p. 9, lines 5-17 and Fig.5 illustrates the PLL module 62 that generates "**CLOCK OUTPUT signal**" (timing output signal) to the downstream radio transceiver (TRX) 52. Clearly, the generated CLOCK OUTPUT signal from the COUNTER/DIVIDER 78 output is the output clock of the PLL module 62 and is the "final" output clock signal (Argument page 3, lines 3-8) as indicated by the applicant. ***The phase detector does not determine successive phase difference value between a reference clock signal and this CLOCK OUTPUT signal (Fig.5 element 78 output)***.

With regard to the "**output clock signal**", specification at p.9 lines 16-17 and Fig.5 describes that **the oscillator 74 generates the "output clock signal"** at a frequency determined by the oscillator control signal.

Specification at p.9 lines 11-13 and Fig.5 further describes that the phase detector 66 receives **a feedback signal driven by the "output clock signal"** produced by the module PLL 62, and generates a phase error signal by determining a phase difference between the reference signal and the feedback signal.

*Clearly, **the "output clock signal" (output of the oscillator 74)** that used to generate the feedback signal (output of COUNTER/DIVIDER 76) **is an internal signal to the PLL module 62**. As addressed in the above paragraph, the NCO 9*

output signal is corresponding to the "output clock signal" (output of the oscillator 74) as recited in Claims 1, 10 and 24.

In summary,

(A) The specification of the instant application at p. 8, lines 14 — 15, p. 8, line 24 — p. 9, line 8, p. 9, lines 5-17 and Fig.5 and p. 9, lines 5-17 and Fig.3-5 as recited by the applicant does not support the Applicant's argument. Applicant has wrongly taken OUTPUT CLOCK signal (Fig.5 COUNTER/DIVIDER 78 output) as that of "the clock output signal" (Fig.5 oscillator 74COUNTER/DIVIDER 76 output) to interpret claim 1 limitation as addressed in the above paragraph.

(B) The phase detector determines successive phase difference value between a reference clock signal and **the output clock signal (output of the oscillator) that is in the internal loop of the PLL**. *The NCO 9 output signal of the Tanaka's reference is corresponding to the "output clock signal"* (output of the oscillator 74) as recited in Claims 1, 10 and 24.

Thus, for the explanation addressed in the above paragraph, the Examiner's response to Applicant's argument and the rejection under 35 U.S.C. 102(b) in the last Final Office Action, 5/10/2006, with Tanaka's reference are adequate.

Please note that the symbol g(nT) shown in Fig.C, page 6 of the last Final Office action, 5/10/2006, should be at the input of NCO 9. Examiner apologizes for the typo and thanks to the Applicant for pointing out this typo.

2. Applicants' argument – Refer to page 10 of the Appeal Brief.

(a) "Nor does Tanaka teach the filter adapting limitation of claim 1. As taught by the specification at p. 9, lines 5-24, ... Thus, Tanaka teaches detecting the change amount of residual AFC frequency error relative to a predetermined time, as a control basis for PLL loop adaptation. Such control cannot be said to anticipate the claimed limitation of adapting a (PLL) loop filter based on averaging the PLL frequency control values output by that loop filter, as is explicitly claimed in claim 1."

Examiner's response – In response this argument, examiner first noted that the specification at p. 9, lines 5-24 recited by the Applicant (page 10, lines 3-10, of the Appeal Brief) does not teach the filter or average operation for control values by the control logic 70. It only describes that the control logic 70 determines when and how to update the loop filter 68 to adjust the filtering performed on the phase error signal and emphasize the control logic operates on the filtered control value rather than on the pre-filtered error signal.

Second, Applicant argues that the control basis of the loop filter as shown in Fig.1 of Tanaka's reference can not be said to anticipate the claimed limitation of adapting a (PLL) loop filter based on averaging the PLL frequency control values output by that loop filter. Examiner respectfully disagrees.

Refers to Fig.1 (Figure C, page 6 of the last Final Office Action, dated 5/10/2006) and column 5 line 42 – column 6 line 6 of the Tanaka's reference. The adjustable loop filter 11 output g(nT) provides successive control values to the delayed element 13 and subtractor 14 and outputs a signal having a function of $\Delta g(nT)$, then the averaging circuit 15 averages the function of $\Delta g(nT)$ signal,

where $\Delta g(nT) = g(nT) - g(nT-T)$ (column 5, equation 8) and g(nT) is the filtered successive phase difference values from loop filter 11 output and g(nT-T) is the delayed successive phase difference values.

The data determining device 16 compares the averaged signal with a threshold and outputs the determined signal to the PLL controller 102 to select the parameters of the loop range, the frequency control width, and the control time interval of the PLL corresponding to the output signal of the data determining unit 16 so as to control the PLL filter 11 (column 5 line 42 – column 6 line 6).

From the teaching of the Tanaka's reference it is clear that the PLL (Fig.1 elements 8-11, 13-16, 101 and 102) circuit adapts a (PLL) loop filter 11 based on averaging (Fig.1 element 15) the PLL frequency control values output (Fig.1 element g(nT)) by that loop filter.

By definition, "based on" means --- to make, form or serve as a basic for --- (Merriam-Webster's College Dictionary, tenth edition, 1998).

Since the loop filter 11 adapting or adjusting process is based on the output signal of the data determining unit 16 that is based on the determination result of the averaged $\Delta g(nT)$ ($\underline{\Delta g(nT) = g(nT) - g(nT-T)}$), it is clear for one of ordinary skill in the art at the time of the invention was made to make conclusion that the loop filter 11 adapting or adjusting process is based on the averaging control values (output of averaging circuit 15) determined from said successive control value (g(nT)).

Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 102(b) with Tanaka's reference is adequate.

Dependent Claims 2-4

1. Applicants' argument – Refer to page 11 of the Appeal Brief.

(a) "The cited sections of Tanaka do not teach averaging the control values output by a PLL loop filter and (b) detecting a trend in that average for loop filter adaptation. Rather, as the cited sections explain, Tanaka teaches a filter element 11 that is updated from a memory element 101 based on elements 13, 14 determining the amount that the output of filter element 11 changes over a predetermined time D (as set by element 13). More particularly, element 15 averages the change amounts, and element 16 uses the average of the change amounts—explicitly not the average of the actual output values from filter element 11—to control which update parameters are retrieved from memory element 101 by the PLL controller 102 to update the filter element 11."

Examiner's response –

With respect to argument (a), the response has been addressed in the above paragraph (claim 1). Although element 16 does not uses the average of the actual output values from filter element 11 to control which update parameters are retrieved from memory element 101 by the PLL controller 102 to update the filter element 11, element 16 outputs the determined signal based on the averaged control values output (g(nT)) to the PLL controller 102 to select the parameters of the loop range, the frequency control width, and the control time interval of the

PLL corresponding to the output signal of the data determining unit 16 so as to control the PLL filter 11 (column 5 line 42 – column 6 line 6).

With respect to argument (b), Tanaka teaches that the output signal of the averaging circuit 15 is supplied to the element 16 to determine whether or not the output signal of the averaging circuit 15 is large toward a threshold level (column 5 lines 55-65). It is clear that determining whether or not the output signal of the averaging circuit 15 is large toward a threshold level is a trend detecting process with respect to said average control values, since by definition, "trend" means "The general direction in which something tends to move."

Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 102(b) with Tanaka's reference is adequate.

Dependent Claims 5-7

1. Applicants' argument – Refer to page 11 – 13 of the Appeal Brief.

(a) "It is self-evident from Tanaka's Figure 1 and from the corresponding descriptions in Tanaka's specification, that subtraction element 14 and delay element 13 cooperate to produce "change amounts," which reflect the amount by which the output of filter element 11 has changed over the predetermined time period D. Those change values are filtered by element 15. The change values are not control values as output by filter element 11, and the averaged change values of Tanaka are not averaged control values within the meaning of applicant's claims. Tanaka therefore does not teach the limitations of claim 5 and therefore cannot anticipate claim 5."

Examiner's response – Applicant's arguments with respect to the rejection(s) of claim(s) 5-7 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

Dependent Claims 13-16 and 18

1. Applicants' argument – Refer to page 16 of the Appeal Brief.

(a) "Tanaka does not teach averaging the control values output by a PLL loop filter as is required in claim 10, and does not teach determining differences in those average control values as is required in claim 13. Moreover, nowhere does Tanaka mention integrating differences in average control values, as is further required in claim 13. "

Examiner's response – Applicant's arguments with respect to the rejection(s) of claim(s) 5-7 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

Dependent Claims 34, 35 and 39

1. Applicants' argument –

(a) "Applicant notes that the examiner does not allege that Wilhelmsson provides any teachings relevant to the PLL **loop** filter output control value averaging and corresponding PLL loop filter adaptations present in independent claim 24, nor does Wilhelmsson provide such teachings. Therefore, with those teachings absent from Tanaka, as argued for the independent claims, the combination of Tanaka with Wilhelmsson cannot render obvious any claims depending from

claim 24. As such, as a matter of law, claims 34, 35, and 39, all depending from independent claim 24, are not obvious over the combination of Tanaka and Wilhelmsson.

(b) "Moreover, regarding claim 39, the examiner rests the obviousness rejection on the assertion that one would combine Wilhelmsson's teachings with Tanaka's because it would reduce board size and therefore reduce circuit cost. As a statement of motivation to combine, that falls far short of the legal requirements for making out *a prima facie* case of obviousness."

Examiner's response –

With respect to argument (a), it is well known in the field of communication art, for an analog PLL circuit, the purpose of a digital-to-analog converter, DAC, (control circuit) is to convert the digital value from the output of loop filter to analog form so that the VCO can be adjusted to a preferred frequency output and locked to the input reference signal. In the other hand, a numerical controlled oscillator, NCO, is a digital form of the PLL circuit. The NCO receives digital value(s) directly from the output of a loop filter and adjusts its output to a preferred frequency for a digital PLL circuit.

Examiner cites Wilhelmssons' reference to show that the DAC (Fig.12 element 3) with input from a digital value generated from said loop filter (Fig.12 element 44) and a VCO controlled by the DAC generated control viltage (Fig.12 element 9) for a PLL circuit is an equivalent structure known in the art to a NCO as that of a digital PLL circuit. Therefore, because these two "the NCO" and "the DAC with VCO" were art-recognized equivalents at the time the invention was

made, one of ordinary skill in the art would have found it obvious to substitute (DAC and VCO) for (NCO). Forthermore, this art-recognized equivalents does not involve the specific type of the loop filter. As long as the loop filter provides digital output to the input of the DAC, the DAC will convert this digital input signal to an analog waveform for further use.

Dependent Claim 39

1. Applicants' argument –

(a) "Moreover, regarding claim 39, the examiner rests the obviousness rejection on the assertion that one would combine Wilhelmsson's teachings with Tanaka's because it would reduce board size and therefore reduce circuit cost. As a statement of motivation to combine, that falls far short of the legal requirements for making out *a prima facie* case of obviousness."

Examiner's response –

With respect to argument (a), Applicant does not define what the digital processor is in the claim and specification of the instant application. In specification page 11, line 11, teaches a digital loop filter 68. The output of the digital filter is submitted to the control logic 70. Since the control logic 70 processes the digital signal from the output of the digital loop filter 68, it is inherent that the control logic comprising a digital device for processing the input digital signal. The digital device for processing the digital signal is considered as a digital processor.

With above interpretaion of the digital processor, Tanaka teaches a control logic (Fig.1 elements 13-16, 101 and 102) comprising a digital processor 14 to subtract a digital signal g(nT) and delayed digital signal g(nT-T) for subtraction operation or processing.

Combination of Wilhelmsson's teachings with Tanaka's as described in the last Final Office action is to show an alternative interpretation of a digital processor, named microprocessor. It is well known in the art that the arithmetic operation, such as subtraction, can be performed by a microprocessor to replace many discrete digital components to save PC board size for cost reduction.

Dependent Claims 12 and 33

1. Applicants' argument –

(a) "First, the proffered motivation to combine is legally insufficient, as it represents mere speculation by the examiner that clock jitter in Tanaka would be improved by incorporation of Glass's teachings. One might just as easily speculate that Tanaka already configures its filter element 11 as a proportional-integral filter, although Tanaka does not disclose such details.

However, even if Tanaka is so modified (or inherently operates in the alleged manner), neither Glass nor Tanaka teach adapting proportional-integral filter coefficients as a function of the average of the control values being output by the filter at issue. Without providing these teachings, the combination of Tanaka and Glass as a matter of law cannot render claim 12 obvious."

Examiner's response – Applicant's arguments with respect to the rejection(s) of claim(s) 12 and 33 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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August 04, 2006

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